Refine Search

Search Results -

Terms	Documents
("machine specific register" or MSR) near10 (SOC or chip or IC)	8

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L1

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, September 28, 2006 **Purge Queries** Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB; PLUR=YES; OP=OR		
L1	("machine specific register" or MSR) near10 (SOC or chip or IC)	8	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
("machine specific register" or MSR) near10 (SOC or chip or IC)	6

Database:
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US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
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Search: L3

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, September 28, 2006 Purge Queries | Printable Copy | Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	("machine specific register" or MSR) near10 (SOC or chip or IC)	6	L3
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L2	L1 same address	3	L2
L1	("machine specific register" or MSR) near10 (SOC or chip or IC)	18	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(709/230 |709/250 |709/238 |709/253 |370/351 |370/416 |370/463 |370/402 |712/32 |712/33 |712/17 |712/28 |712/208 |710/104 |710/309 |710/105 |710/5 |710/33 |710/20 |710/38 |710/100 |710/305 |711/2 |711/202 |711/220).ccls.	19259

Database:
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- US OCR Full-Text Database
- EPO Abstracts Database
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Search: L4

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, September 28, 2006 Purge Queries Printable Copy Create Case

Set Name	Query
side by side	
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR
L4	710/104,309,105,5,33,20,38,100,305;709/230,250,238,253;370/351,416,463,402;712/32,33,17,28
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
L3	("machine specific register" or MSR) near10 (SOC or chip or IC)
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR
L2	L1 same address
L1	("machine specific register" or MSR) near10 (SOC or chip or IC)

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L4 and L5	10

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Thursday, September 28, 2006 Purge Queries Printable Copy Create Case

Set Name side by side	Query
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR
L6	l4 and L5
L5	("machine specific register" or MSR) same (SOC or chip or IC)
L4	710/104,309,105,5,33,20,38,100,305;709/230,250,238,253;370/351,416,463,402;712/32,33,17,28
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
L3	("machine specific register" or MSR) near10 (SOC or chip or IC)
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR
L2	L1 same address
L1	("machine specific register" or MSR) near10 (SOC or chip or IC)

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
path same address same ("machine specific register" or MSR) same writ$3	2

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

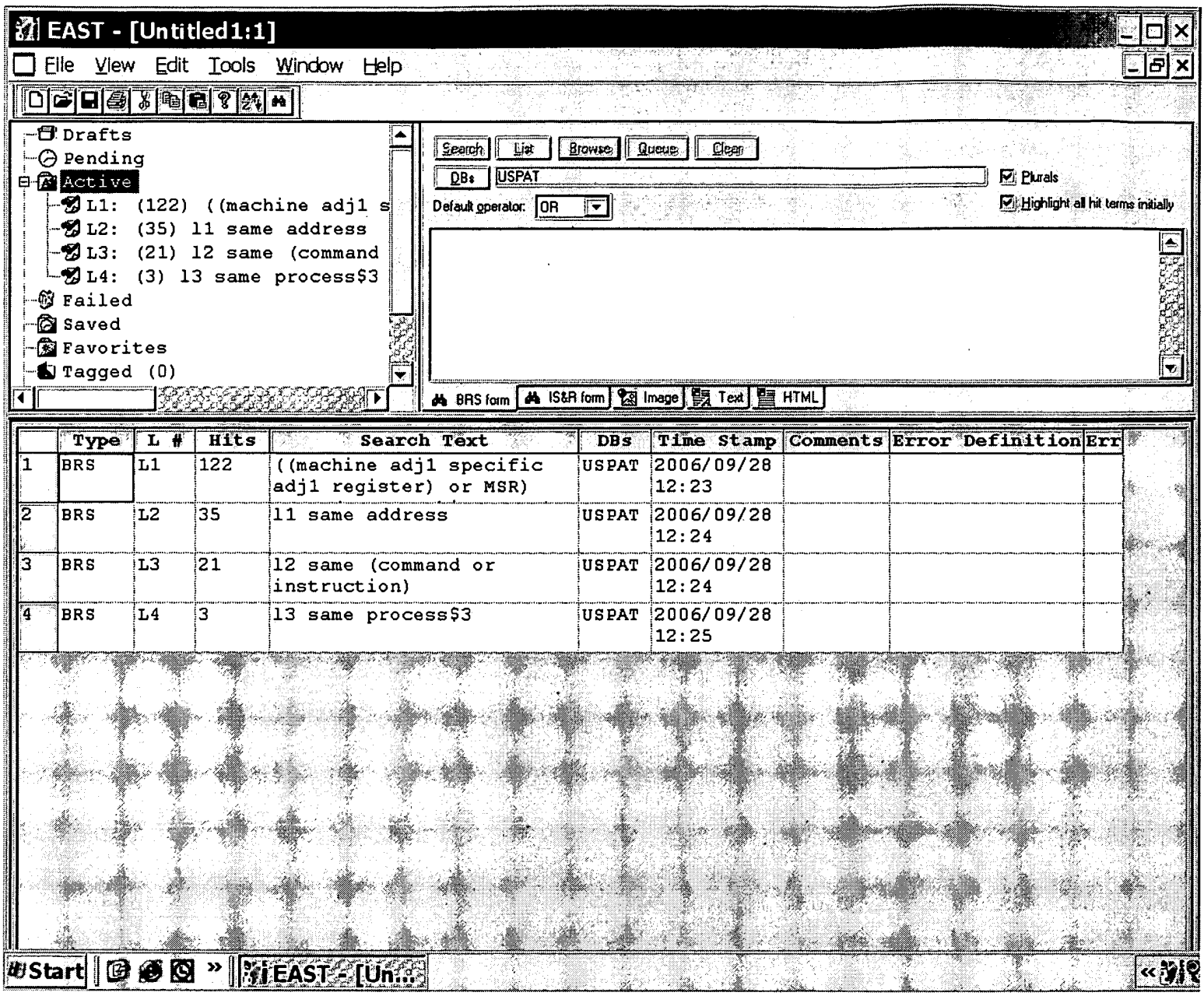
Refine Search | Recall Text | Clear | Interrupt

Search History

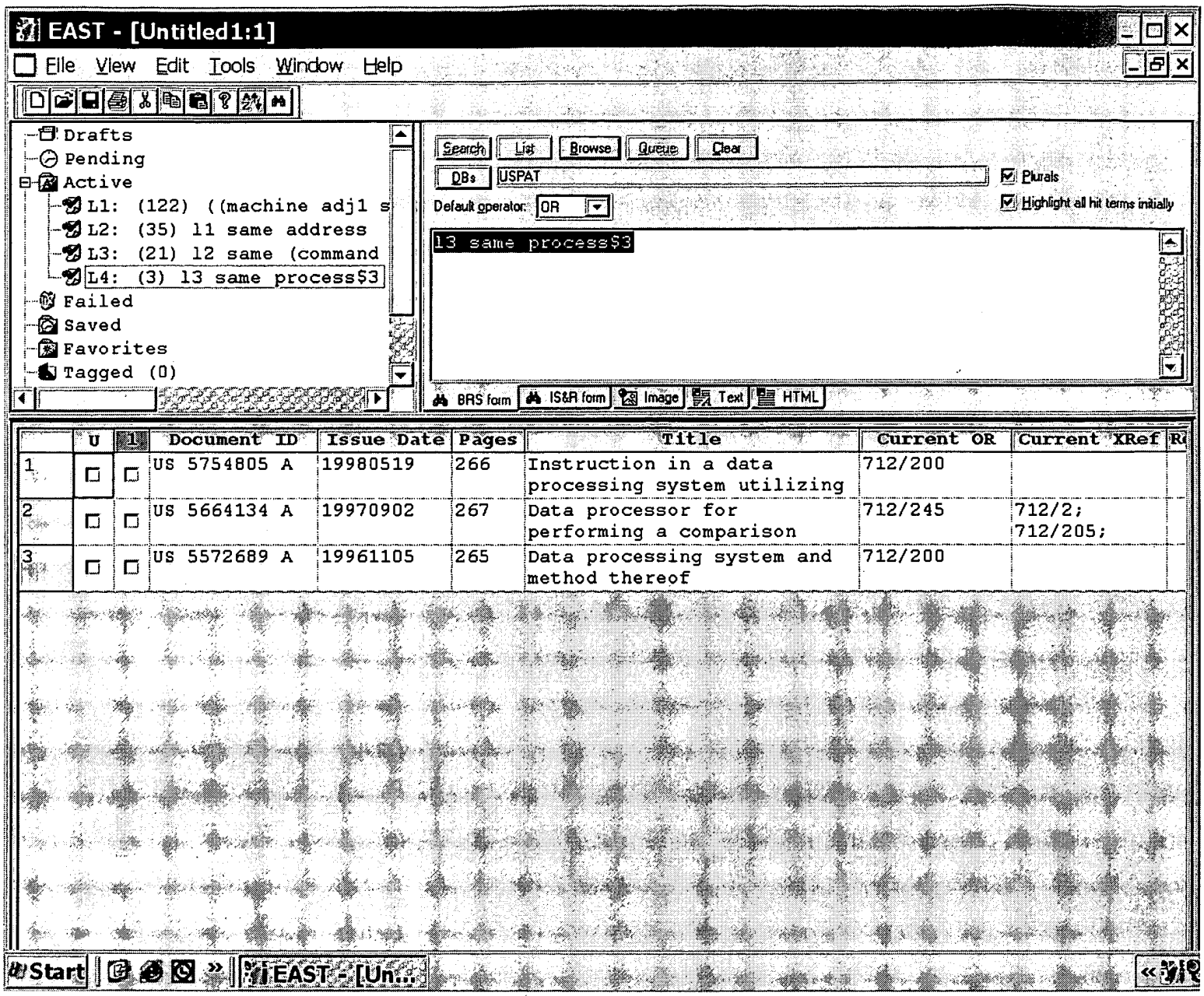
DATE: Thursday, September 28, 2006 Purge Queries | Printable Copy | Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	path same address same ("machine specific register" or MSR) same writ$3	2	L2
L1	path same address same ("machine specific register" or MSR) same writ$3 same port	0	L1

END OF SEARCH HISTORY



	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	122	((machine adj1 specific adj1 register) or MSR)	USPAT	2006/09/28 12:23			
2	BRS	L2	35	l1 same address	USPAT	2006/09/28 12:24			
3	BRS	L3	21	l2 same (command or instruction)	USPAT	2006/09/28 12:24			
4	BRS	L4	3	l3 same process$3	USPAT	2006/09/28 12:25			


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (122) ((machine adj1 s
L2: (35) l1 same address
L3: (21) l2 same (command
L4: (3) l3 same process$3
Failed
Saved
Favorites
Tagged (0)
Search List Browse Queue Clear
DBs USPAT
Plurals
Default operator: OR
Highlight all hit terms initially
l3 same process$3
BRS form IS&R form Image Text HTML
U 1 Document ID Issue Date Pages Title Current OR Current XRef
1 US 5754805 A 19980519 266 Instruction in a data processing system utilizing 712/200
2 US 5664134 A 19970902 267 Data processor for performing a comparison 712/245 712/2; 712/205;
3 US 5572689 A 19961105 265 Data processing system and method thereof 712/200
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EAST - [Un...

Results for "((register<in>metadata) <and> (chip<in>metadata))<and> (command<in..." e-mail
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Volume 45, Issue 3, Part 1, June 1998 Page(s):849 - 851
Digital Object Identifier 10.1109/23.682649
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2. **An 800-MHz embedded DRAM with a concurrent refresh mode**
Kirihata, T.; Parries, P.; Hanson, D.R.; Hoki Kim; Golz, J.; Fredeman, G.; Rajeı
Griesemer, J.; Robson, N.; Cestero, A.; Khan, B.A.; Geng Wang; Wordeman, M
Solid-State Circuits, IEEE Journal of
Volume 40, Issue 6, June 2005 Page(s):1377 - 1387
Digital Object Identifier 10.1109/JSSC.2005.848019
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An 800-MHz embedded DRAM with a concurrent refresh mode

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Technol. Group, IBM Syst., Hopewell Junction, NY, USA

This paper appears in: **Solid-State Circuits, IEEE Journal of**
Publication Date: June 2005
Volume: 40 , Issue: 6
On page(s): 1377 - 1387
ISSN: 0018-9200
INSPEC Accession Number:8459799
Digital Object Identifier: 10.1109/JSSC.2005.848019
Posted online: 2005-06-13 13:09:05.0

Abstract
An 800-MHz embedded DRAM macro employs a memory cell utilizing a device from the 90-nm high-performance technology menu; a 2.2-nm gate oxide 1.5 V IO device. A concurrent refresh mode is designed to improve the memory utilization to over 99% for a 64 /spl mu/s data retention time. A concurrent refresh scheduler utilizes up-count and down-count **registers** to identify at least one array to be refreshed at every clock cycle, emulating a classical distributed refresh mode. A **command** multiplier employs low frequency phased clock signals to generate the clock, **commands**, and addresses at rates up to 4/spl times/ that of the tester frequency. The macro integrates masked redundancy allocation logic during at speed multibank test. The hardware results show a 312-MHz random access frequency and 800-MHz multibank frequency at 1.2 V, respectively.

Index Terms
Inspec

Controlled Indexing
DRAM **chips** UHF integrated circuits multiplying circuits nanoelectronics shift **registers**

Non-controlled Indexing
1.2 V 1.5 V 2.2 nm 312 MHz 800 MHz 90 nm **command** multiplier concurrent refresh mode concurrent refresh scheduler down-count **registers** embedded DRAM high-performance cell low frequency phased clock signals masked redundancy allocation logic

memory cell random access frequency speed multibank test up-count **registers**

Author Keywords

Command multiplier concurrent refresh mode embedded DRAM high-performance cell refresh scheduler

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